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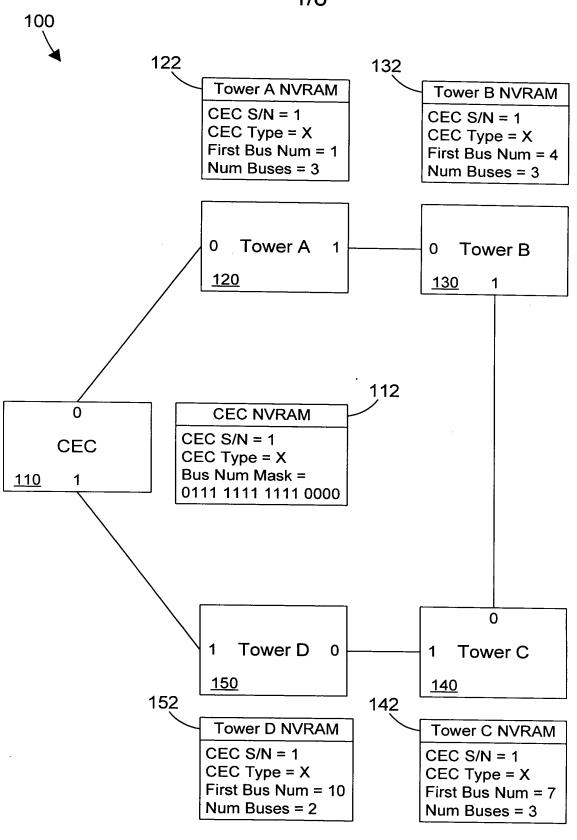


FIG. 1 Prior Art

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2/8 128 Tower A 138 Tower B > 138. S S S S S S S S $\overline{\mathsf{s}}$ S S S L L L L O 0 0 0 0 0 0 0 0 0 O 0 Т T T Т T Т T T T T Т PHB PHB PHB **PHB** PHB PHB 126 <u>126</u> 126 <u>136</u> <u>136</u> 136 NV **RIO Bus** NV **RIO Bus** Adapter **RAM** -124 Adapter RAM 134 **-122** 0 **\132** 110 120 130 119 CEC 118 116 Memory Bus # **CPUs** Manager 114 NV 0 **RIO Hub RAM -112** 1 150 140 - 152 0 142 0 154 144 **RIO Bus** NV NV **RIO Bus** Adapter **RAM** RAM Adapter PHB PHB PHB PHB PHB 156 156 <u>146</u> <u>146</u> 146 S S S S S S S S L L L L L L L 0 0 O 0 0 0 0 0 0 0 T T T Т Т Т Т Т Т Т

FIG. 2 Prior Art

Tower C

148

148

Tower D

158

158

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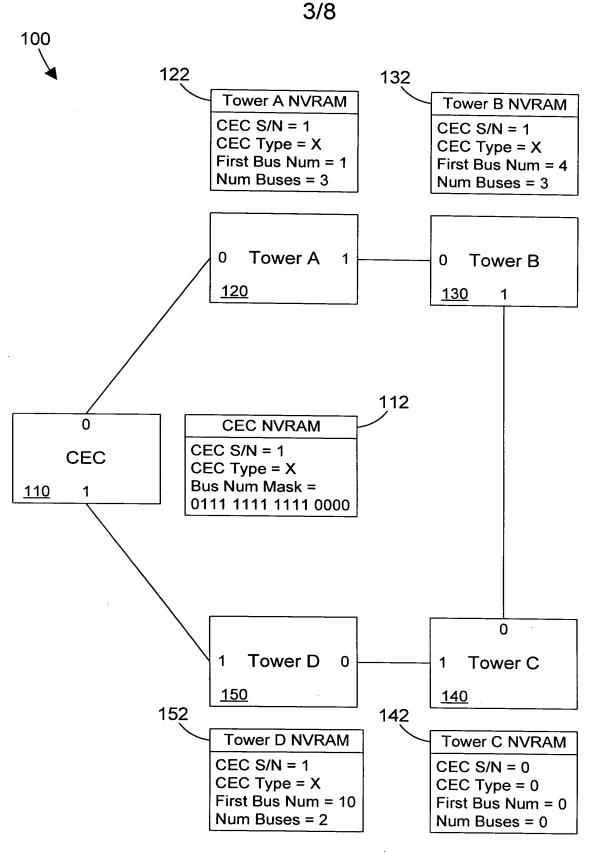


FIG. 3 Prior Art

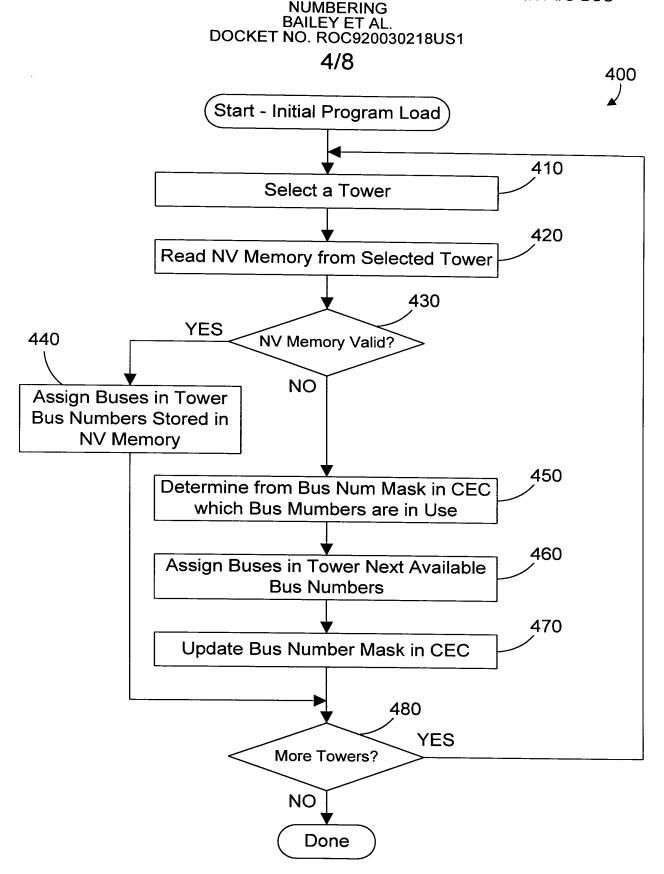


FIG. 4 Prior Art

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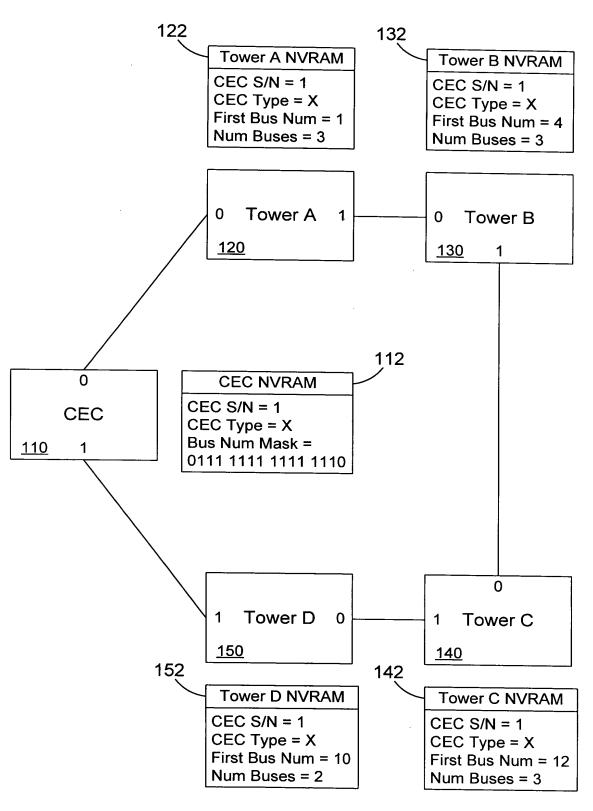
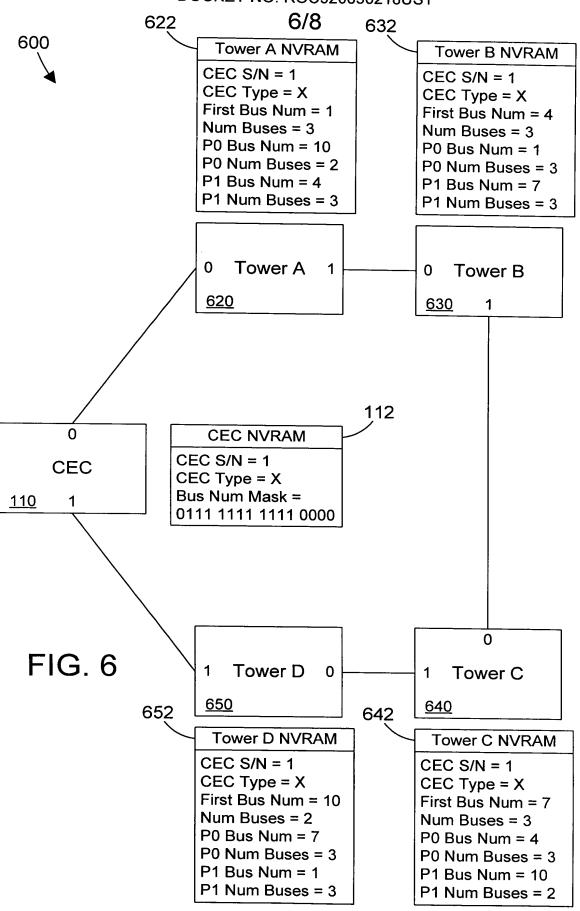


FIG. 5 Prior Art

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